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TITLE: METHODO OF PRODUCING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE

Hon. Commissioner for Patents,

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SIR;

CERTIFIED TRANSLATION

I, Yasuo OKUZAWA, am an official translator of the Japanese language into the English language and I hereby certify that the attached comprises an accurate translation into English of Japanese Application No. 2003-084475, filed on March 26, 2003.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Yasuo Okuzawa

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[TITLE OF THE INVENTION] SEMICONDUCTOR DEVICE AND METHOD OF PRODUCING SAME

[CLAIMS]

[Claim 1]

A semiconductor device comprising a plurality of electronic elements, electrodes of the plurality of electronic elements being formed on a semiconductor substrate, and insulating films between the electrodes and the semiconductor substrate differing in required electrical effective thickness, wherein

concentrations of impurities of the electrodes are determined so that the concentrations of the impurities of the electrodes differ for each electronic element according to the required electrical effective thickness of the insulating film and the effective thickness is controlled by depletion of the electrodes due to the concentrations of the impurities.

[Claim 2]

A semiconductor device as set forth in claim 1, wherein said electronic elements include a plurality of transistors having said electrodes as gate electrodes and said insulating films as gate insulating films.

[Claim 3]

A semiconductor device as set forth in claim 1,

wherein the plurality of said electronic elements include a transistor having said electrode as gate electrode and said insulating film as gate insulating film and a capacitor having said electrode as a capacitive electrode and said insulating film as said a capacitive insulating film.

[Claim 4]

A method of producing a semiconductor device for forming gate electrodes of a plurality of transistors supplied with different voltages on a semiconductor substrate via a gate insulating film, comprising the steps of:

forming said gate insulating film on said semiconductor substrate;

forming a gate electrode layer containing an impurity on said gate insulating film;

implanting an impurity at regions of said gate electrode layer for forming transistors where the electrical effective thickness required for said gate insulating film based on said voltage is relatively thin; and

processing said gate electrode layer to form gate electrodes with concentrations of impurities differing for each transistor.

[Claim 5]

A method of producing a semiconductor device as set forth in claim 4, wherein the step of forming said gate electrode layer comprises the steps of:

forming an amorphous silicon layer on said gate insulating film and

implanting an impurity in said amorphous silicon layer.

[Claim 6]

A method of producing a semiconductor device as set forth in claim 4, wherein the step of forming said gate insulating film comprises forming on said semiconductor substrate said gate insulating films with different thicknesses between region for forming transistor having relatively thin effective thickness required for said gate insulating film and region for forming transistor having relatively thick effective thickness required for said gate insulating film.

[Claim 7]

A method of producing a semiconductor device for forming gate electrode of transistor and upper capacitive electrode via insulating films on a semiconductor substrate, comprising the steps of:

forming lower electrode of said capacitor in said semiconductor substrate;

forming an insulating film to be a gate insulating

film of said transistor and a capacitive insulating film of said capacitor in the semiconductor substrate;

forming an electrode layer containing an impurity to be said gate electrodes or said capacitive electrode later on said insulating film;

implanting an impurity at regions of said electrode layer for forming transistor where the effective thickness required for said insulating film is relatively thin compared with said capacitor; and

processing said electrode layer to form said gate electrode and said capacitive electrode having different concentrations of impurities.

[Claim 8]

A method of producing a semiconductor device as set forth in claim 7, wherein the step of forming said lower electrodes comprises the steps of:

forming a sacrificial film in said semiconductor substrate;

implanting the impurity via said sacrificial film in region of said semiconductor substrate for forming said capacitor so as to form said lower electrode; and

removing said sacrificial film.

[Claim 9]

A method of producing a semiconductor device as set forth in claim 7, wherein the step of forming said

electrode layer comprises the steps of:

forming an amorphous silicon layer on said insulating film and

implanting an impurity in said amorphous silicon layer.

[Claim 10]

A method of producing a semiconductor device as set forth in claim 7, wherein the step of forming said gate insulating film comprises forming said insulating film with different thicknesses between region for forming the gate insulating film of said transistor and region for forming capacitive insulating film of said capacitor.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Technical Field of the Invention]

The present invention relates to a semiconductor device and to a method of producing a semiconductor device, more particularly relates to a semiconductor device having MOS transistors, capacitors, or other different types of elements with different power source voltages formed on a same substrate and to a method of producing thereof.

[0002]

[Prior Art]

Recently, in general, in LSI processes, circuits are

being made higher in integration and elements are being miniaturized more. Along with this, it is required that MOS transistors, capacitors, resistance elements, and other different types of devices of types of different power source voltages are simultaneously formed on the same substrate as much as possible without increasing the number of steps.

[0003]

Further, to improve the performance of MOS transistors, more miniaturization is required. Along with the drop in the power source voltage due to this, gate oxide films are also being made thinner. Even if the main MOS transistors are formed by thin films, the MOS transistors supplied with high voltages used for example for I/O parts, analog circuits, etc. require thicker oxide films commensurate with those power source voltages.

[0004]

Regarding such MOS transistors having different source voltages, the general practice is to form separate gate oxide films physically. As an example of a method of formation, for example, a heat oxide film is formed on a semiconductor substrate, a photo resist or other mask is formed only on regions for forming a device using a thick gate oxide film, and the other parts of the heat oxide film are removed by performing a wet etching using a

hydrofluoric acid solution etc. After the resist is removed, the semiconductor substrate is heat oxidized a second time to form a heat oxide film. As a result, gate oxide films having different thicknesses are formed.

[0005]

With the above method, by repeating the photo resist patterning step, the wet-etching step, and the heat-oxidation step, it is possible to obtain as many different types of thicknesses of heat oxide films as desired.

[0006]

Further, in the past, the technique of simultaneously forming capacitors when forming MOS transistors has been used. As the method of formation, for example, a semiconductor substrate is doped with a high concentration of ions through a suitable sacrificial oxide film to make the silicon substrate an n+ or p+ type and form one capacitive electrode. After the sacrificial film is removed, heat oxidation is used to form a capacitive oxide film of the capacitor with desired oxide film thickness at the same time as the gate oxide film of the MOS transistor. In the above oxidation step, the oxidation treatment proceeds faster than normal due to crystal defects formed in the substrate by the ions previously implanted at a high concentration (accelerated

oxidation). As a result, the capacitive oxide film of the capacitors becomes thicker than the gate oxide film. As following steps, polycrystalline silicon is deposited and patterned so as to form the other capacitive electrode at the same time as gate electrode of the MOS transistor.

[0007]

With the above method, it is possible to efficiently form the capacitor on the same substrate at the same time as the MOS transistor without greatly increasing the number of steps.

[0008]

On the other hand, it is known that by making the concentration of impurities in a gate electrode high, depletion under the gate electrodes is prevented (refer to patent article 1).

[0009]

[patent article 1]

Japanese Unexamined Patent Publication (Kokai) No. 2000-277636

[0010]

[Problem to be Solved by the Invention]

In the case of the above method for forming separate oxide films physically, however, at first there is a problem that the number of steps increased along with the number of types of thicknesses of the oxide films.

Further, at the time of performing the wet etching, the hydrofluoric acid solution etc. infiltrated the portion corresponding to the edges of the masked oxide film and ends up damaging the oxide film supposed to remain. This may influence the elements and lower the reliability. Therefore, it is not preferable to use these methods frequently.

[0011]

In case of the method of formation of capacitors, the silicon substrate is doped with ions to a high concentration to form the electrodes. To obtain the desired capacity, it may be to promote accelerated oxidation to obtain a thick oxide film able to withstand a high voltage. However, if implanting ions at a particularly high concentration to promote accelerated oxidation, the damage given to the silicon substrate becomes greater, therefore the quality of the oxide film is lowered and the reliability ends up being reduced. Further, the ratio of poor quality film due to the accelerated oxidation increases and becomes a cause of a drop in reliability.

[0012]

As explained above, raising the performance of the main MOS transistors of an LSI requires that the thickness of the gate oxide film is made physically thin.

This oxide film has to maintain the thin electrical effective thickness of the oxide film when operating the transistors as it is. Therefore, it is necessary to satisfy the requirements of all of the thin film transistors, transistors with different power sources, capacitors, and other elements requiring different oxide film thicknesses.

[0013]

The present invention is made under the above circumstance and a first object of the present invention is to provide a semiconductor device able to secure electrical effective thicknesses required for insulating films of electronic elements by using depletion of electrodes of the electronic elements even if the physical thicknesses of the insulating films are not different.

A second object of the present invention is to provide a method of producing a semiconductor device able to secure electrical effective thicknesses required for gate insulating films of transistors and capacitive insulating films of capacitors while keeping down the increase in number of steps due to the formation of separate insulating films with physically different thicknesses.

[0014]

[Means for Solving the Problem]

To achieve the first object, according to a first aspect of the invention, there is provided a semiconductor device having a plurality of electronic elements, electrodes of the plurality of electronic elements being formed on a semiconductor substrate, and insulating films between the electrodes and the semiconductor substrate differing in required electrical effective thickness, wherein concentrations of impurities of the electrodes are determined so that the concentrations of the impurities of the electrodes differ for each electronic element according to the required electrical effective thickness of the insulating film and the effective thickness is controlled by depletion of the electrodes due to the concentrations of the impurities.

[0015]

The plurality of the electronic elements include a plurality of transistors having the electrodes as gate electrodes and the insulating films as gate insulating films.

[0016]

The plurality of the electronic elements include a transistor having the electrode as gate electrode and the insulating film as gate insulating film and a capacitor having the electrode as a capacitive electrode and the

insulating film as the a capacitive insulating film.

[0017]

According to the semiconductor device of the present invention, the concentrations of impurities of the electrodes are determined so that the concentrations of the impurities of the electrodes differ for each electronic element according to the required electrical effective thickness of the insulating film. Therefore, the effective thickness is controlled by depletion of the electrodes due to the concentrations of impurities.

[0018]

To achieve the second object, according to a second aspect of the invention, there is provided a method of producing a semiconductor device for forming gate electrodes of a plurality of transistors supplied with different voltages on a semiconductor substrate via a gate insulating film, having the steps of forming the gate insulating film on the semiconductor substrate, forming a gate electrode layer containing an impurity on said gate insulating film, implanting an impurity at regions of the gate electrode layer for forming transistors where the electrical effective thickness required for the gate insulating film based on the voltage is relatively thin, and processing the gate electrode layer to form gate electrodes with

concentrations of impurities differing for each transistor.

[0019]

According to the method of producing a semiconductor device of the present invention, an impurity is implanted into the regions of the gate electrode layer for forming transistors where the effective thickness of the gate insulating films based on the power source voltage able to be supplied is relatively thin. Therefore, a gate electrode processed from the gate electrode layer in a region where no impurity was introduced at this time has a relatively low concentration of impurity, so the effective thickness of the gate insulating film becomes thicker due to depletion of the gate electrode. On the other hand, a gate electrode in which the above impurity was introduced has a relatively high concentration of impurity, so depletion of the gate electrode is prevented and the electrical effective thickness is kept thin.

[0020]

Further, to achieve the second object, according to a third aspect of the invention, there is provided a method of producing a semiconductor device for forming gate electrode of transistor and upper capacitive electrode via insulating films on a semiconductor substrate, having the steps of forming lower electrode of

the capacitor in the semiconductor substrate, forming an insulating film to be a gate insulating film of the transistor and a capacitive insulating film of the capacitor in the semiconductor substrate, forming an electrode layer containing an impurity to be the gate electrodes or the capacitive electrode later on the insulating film, implanting an impurity at regions of the electrode layer for forming transistor where the effective thickness required for the insulating film is relatively thin compared with the capacitor, and processing the electrode layer to form the gate electrode and the capacitive electrode having different concentrations of impurities.

[0021]

According to the method of producing a semiconductor device of the present invention, an impurity is implanted at regions of the electrode layer for forming transistor where the effective thickness required for the insulating film is relatively thin compared with the capacitor. Therefore, a capacitive electrode processed from the electrode layer in a region where no impurity was introduced at this time has a relatively low concentration of impurity, so the effective thickness of the capacitive insulating film becomes thicker due to depletion of the capacitive electrode. On the other hand,

a gate electrode in which the above impurity was introduced has a relatively high concentration of impurity, so depletion of the gate electrode is prevented and the electrical effective thickness is kept thin.

[0022]

[Embodiment of the Invention]

Hereinafter, semiconductor devices and methods of producing the same of embodiments of the present invention will be described with reference to the drawings.

[0023]

First Embodiment

FIG. 1 is a cross-sectional view of a semiconductor device according to the present invention. As shown in FIG. 1, a semiconductor substrate 1 having, for example, silicon is formed with an element-isolation insulating film 2 of silicon oxide defining active regions. The active regions of the semiconductor substrate 1 are formed with two transistors Tr1 and Tr2 to which different power source voltages are supplied. The transistor Tr1 is used as a transistor to which a high power source voltage is supplied, while the transistor Tr2 is made a high performance transistor having high speed and large drive current.

[0024]

That is, gate electrodes 4a and 4b of the transistors Tr1 and Tr2 are formed on the semiconductor substrate 1 via gate insulating films 3. The side parts of the gate electrodes 4a and 4b are formed with sidewall insulating films 5 of for example silicon oxide. In this embodiment, the physical thicknesses of the gate electrodes 3 of the transistors Tr1 and Tr2 are substantially the same. The gate electrode 4a is formed by a polycrystalline silicon layer containing an impurity in a relatively low concentration, and the gate electrode 4b is formed by a polycrystalline silicon layer containing an impurity in a relatively high concentration.

[0025]

n- semiconductor regions 6a in which an impurity is introduced at a low concentration are formed in the semiconductor substrate 1 directly under the sidewall insulating films 5 of the transistors Tr1 and Tr2, while n+ semiconductor regions 6b in which an impurity is introduced at a high concentration compared with the n- semiconductor regions 6a are formed in the semiconductor substrate 1 at the outside of the semiconductor regions 6a. In this way, source/drain regions 6 of lightly doped drain (LDD) structures are formed from the n- semiconductor regions 6a and the n+ semiconductor regions 6b.

[0026]

In the semiconductor device according to the present embodiment, since the gate electrode 4a of the high withstand voltage use transistor Tr1 to which a high power source voltage is supplied contains an impurity at a relatively low concentration, depletion of the gate electrode 4a easily occurs when supplying the gate voltage. This depletion of the gate electrode 4a is equivalent to increasing the thickness of the gate insulating film 3. The high withstand voltage use transistor Tr1 requires a large film thickness of the gate insulating film 3. By utilizing the depletion of the gate electrode 4a, it is possible to make the electrical effective thickness required from the gate insulating film 3 thicker.

[0027]

On the other hand, the gate electrode 4b of the high performance transistor Tr2 required to have a high speed and large drive current contains an impurity in a relatively high concentration so that depletion of the gate electrode 4b does not occur. As a result, the electrical effective thickness of the gate insulating film 3 is also kept thin. Therefore, it is possible to prevent obstruction of the high speed operation caused by depletion of the gate electrode and realize a high speed

and large drive current.

[0028]

Next, a method of producing a semiconductor device according to the present embodiment will be described with reference to FIG. 2 to FIG. 4.

[0029]

First, as shown in FIG. 2(a), a semiconductor substrate 1 wherein active regions are determined by an element-isolation insulating film 2 formed by local oxidation of silicon (LOCOS) or shallow trench isolation (STI) is formed with a gate insulating film 3 of, for example, about 2 nm by heat oxidation. The oxidation conditions at this time are determined so that the oxide film thickness becomes a thin film suitable for the elements requiring the highest performance.

[0030]

Next, as shown in FIG. 2(b), an amorphous silicon film 4-1 is formed. The thickness of the silicon film 4-1 is made for example about 50 to 200 nm. Next, gate ions are implanted for forming an n+ electrode. The gate ion implantation is for example implantation of P by an implantation energy of 20 keV and a dosage of 1 x 1015 cm-2. The dosage at this time is set to a concentration facilitating gate depletion for an element where a thick gate insulating film is required such as a transistor Tr1

for a high power source voltage.

[0031]

Next, as shown in FIG. 3(c), a resist R1 opened at a region including the gate electrode of the transistor Tr2 from which the highest performance is sought is patterned. Using this resist R1 as a mask, addition gate ions are implanted. Therefore, a silicon film 4-2 containing an impurity at a high concentration is formed. This additional gate ion implantation is for example implantation of P at an implantation energy of 20 keV and a dosage of 3 x 1015 cm-2. The dosage at this time is set to one of a concentration high enough to make gate depletion difficult so as to prevent the electrical effective thickness of the gate insulating film required of the transistor Tr2 where the highest performance is sought from becoming greater. After the resist R1 is removed, the introduced impurity is activated by heating. Due to the heat treatment, the amorphous silicon films 4-1 and 4-2 become polycrystalline silicon.

[0032]

Next, as shown in FIG. 3(d), the parts for forming the gate electrodes of the transistors Tr1 and Tr2 are masked by a resist R2, then, as shown in FIG. 4(e), the silicon films 4-1 and 4-2 are dry-etched using the resist R2 as a mask. After that, the resist R2 is removed. Due

to this, the gate electrode 4a of the silicon film 4-1 containing an impurity at a low concentration and the gate electrode 4b of the silicon film 4-2 containing an impurity at a high concentration by two ion implantations are formed.

[0033]

Next, as shown in FIG. 4(f), using the gate electrodes 4a and 4b as a mask, ions of an n-type impurity such as P are implanted at a low concentration to form an n- semiconductor region 6a. By depositing and etching back a silicon oxide film, sidewall insulating films 5 are formed at the side parts of the gate electrodes 4a and 4b.

[0034]

As subsequent steps, using the gate electrodes 4a and 4b and the sidewall insulating films 5 as a mask, an n-type impurity, for example, P, is implanted to a high concentration compared so as to form an n+ semiconductor region 6b. Due to this, source/drain regions 6 having LDD structures are formed. By removing the gate insulating films 3 on the source/drain regions 6, the semiconductor device shown in FIG. 1 is produced.

[0035]

According to the method of producing a semiconductor device according to the present embodiment, since the

gate electrode 4a of the high withstand voltage use transistor Tr1 is formed using a silicon film 4-1 formed by the first gate ion implantation, depletion of the gate electrode readily occurs and a gate insulating film 3 having a thicker electrical effective thickness can be obtained. Further, since the gate electrode 4b of the transistor Tr2 from which a high performance is required is formed by using a silicon film 4-2 obtained a second additional high concentration ion implantation, the electrical effective thickness of the gate insulating film 3 can be kept thin. Therefore, the different types of transistor Tr1 and Tr2 can be formed simultaneously and efficiently on the same substrate while maintaining the capabilities of the transistors.

[0036]

Second Embodiment

In this embodiment, a semiconductor device having transistors and capacitors formed on the same substrate will be explained. Components the same as those of the first embodiment are assigned the same notations and explanations thereof are omitted. FIG. 3 is a cross-sectional view of a semiconductor device according to second embodiment.

[0037]

As shown in FIG. 5, one active region of the

substrate 1 is formed with a high performance transistor Tr2 having a high speed and large drive current. The other active region is formed with a capacitor Ca. The capacitor Ca includes a lower electrode 7 formed on the semiconductor substrate 1 and having a high concentration of the n-type impurity, a capacitive insulating film 3c formed on the lower electrode 7, and an upper electrode (capacitive electrode) 4c formed on the capacitive insulating film 3c.

[0038]

In the present embodiment, the gate insulating film 3b of the transistor Tr2 and the capacitive insulating film 3c of the capacitor Ca are formed simultaneously. Their physical thicknesses are substantially the same. The gate electrode 4b of the transistor Tr2 is formed by a polycrystalline silicon layer containing the impurity in a relatively high concentration. The upper electrode 4c of the capacitor Ca is formed by a polycrystalline silicon layer containing the impurity in a relatively low concentration. The gate electrode 4b and the upper electrode 4c are formed simultaneously.

[0039]

In the semiconductor device according to the present embodiment, since the upper electrode 4c of the high withstand voltage use capacitor Ca designed for the

capacitor voltage includes the impurity in a relatively low concentration, depletion of the upper electrode 4c easily occurs at the time of application of voltage in this structure. The depletion of the upper electrode 4c is equivalent to making the thickness of the capacitive insulating film 3c thicker. The capacitor Ca is required to have a thickness of the capacitive insulating film thicker enough to be able to withstand a high voltage. By utilizing the depletion of the capacitive electrode 4c, the electrical effective thickness required of the capacitive insulating film 3c can be made thicker.

[0040]

On the other hand, the gate electrode 4b of the high performance transistor Tr2 from which a high speed and large drive current are required includes the impurity at a high concentration so that depletion of the gate electrode 4b does not occur, so the electrical effective thickness of the gate insulating film 3b is kept thin. Therefore, it is possible to prevent obstruction of the high speed operation due to depletion of the gate electrode and possible to realize a high speed and large drive current.

[0041]

Next, a method of producing a semiconductor device according to the present embodiment will be described

referring to FIG. 6 to FIG. 9.

[0042]

First, as shown in FIG. 6(a), a semiconductor substrate 1 wherein active regions are determined by an element-isolation insulating film 2 formed by LOCOS or STI is formed with a sacrificial film 8 of silicon oxide by heat oxidation. The thickness of the sacrificial film 8 is for example about 8 nm. Next, a resist R3 opening at the capacitor formation region is patterned. By implanting ions using this resist R3 as a mask, a bottom electrode 7 is formed. The dosage at this time is one sufficient for conversion to an n+ or p+ form, but not increasing the gate leakage current or increasing the crystal defects and lowering reliability. For example, As ions are implanted at an implantation energy of 70 keV and a dosage of 1 x 1015 cm-2.

[0043]

Next, as shown in FIG. 6(b), the resist film R3 is removed and the sacrificial film 8 is removed by a hydrofluoric acid solution. The insulating film 3 for forming the capacitive insulating film of the capacitor Ca and a gate insulating film of the later formed transistor Tr2 is formed by heat oxidation. The oxidation conditions at this time are set so that the oxide film thickness becomes a thin film suitable for the transistor

Tr2 for which the highest performance is required. Next, an amorphous silicon film 4-1 is formed. The thickness of the silicon film 4-1 is for example about 50 to 200 nm. Further, ions are implanted to form an n+ electrode. This ion implantation is implantation of P by an implantation energy of 20 keV and a dosage of 1 x 1015 cm-2. The dosage at this time is made low concentration so that gate depletion becomes easier for an element for which a thick electrical capacitive insulating film is required such as a capacitor Ca for a high power source voltage.

[0044]

The following steps are the same as the steps from FIG. 3(c) explained in the first embodiment. That is, as shown in FIG. 7(c), a resist R4 opening at the region including the gate electrode of the transistor Tr2 from which a high performance is sought is patterned. Using this resist R4 as a mask, additional ions are implanted. Due to this, a silicon film 4-2 containing an impurity at a high concentration is formed. The detailed conditions of the additional gate ion implantation are similar to those of the additional gate ion implantation of the first embodiment. The resist R4 is removed, then the implanted impurity is activated by heat treatment. Due to this heat treatment, the amorphous silicon films 4-1 and 4-2 become polycrystalline silicon.

[0045]

Next, as shown in FIG. 7(d), the part for forming the gate electrode of the transistor Tr2 and the part for forming the upper electrode of the capacitor Ca are masked by a resist R5, then, as shown in FIG. 8(e), the silicon films 4-1 and 4-2 are dry-etched using the resist R5 as a mask. After that, the resist R5 is removed. Due to this, the upper electrode 4c of the silicon film 4-1 containing an impurity at a low concentration and the gate electrode 4b of the silicon film 4-2 formed by two ion implantations and containing an impurity in high concentration of the impurity are formed.

[0046]

Next, as shown in FIG. 8(f), in the state masking the capacitor formation region by a resist, an n-type impurity, for example P, is implanted at the transistor formation region at a low concentration using the gate electrode 4b as a mask to form an n- semiconductor region 6a. The resist is removed, then for example a silicon oxide film is deposited and etched back to form sidewall insulating films 5 at the side parts of the gate electrode 4b.

[0047]

As the following steps, in the state masking the capacitor formation region by a resist, an n-type

impurity, for example P, is implanted at the transistor formation region at a high concentration using the gate electrode 4b and the sidewall insulating film 5 as a mask to form an n+ semiconductor region 6b. Due to this, a source/drain region 6 having an LDD structure is formed. The exposed parts of the insulating film 3 are removed to form the gate insulating film 3b of the transistor Tr2 and the capacitive insulating film 3c of the capacitor Ca, whereby the semiconductor device shown in FIG. 5 is produced.

[0048]

According to the method of producing a semiconductor device according to the present embodiment, by forming a capacitor having the upper electrode 4c formed by the silicon film 4-1 obtained by the first low concentration gate ion implantation, depletion of the upper electrode easily occurs and it is possible to obtain a capacitive insulating film 3c having the thick electrical effective thickness. Further, since the gate electrode 4b of the transistor Tr2 from which a high performance is required is formed by using the silicon film 4-2 additionally implanted with ions to a high concentration a second time, the thin electrical effective thickness of the gate insulating film 3 is maintained as thin. Therefore, it is possible to efficiently and simultaneously prepare

capacitors using different power source voltages on the same substrate while maintaining the capacity of the high performance transistor Tr2.

[0049]

Third Embodiment

FIG. 9 is a cross-sectional view of a semiconductor device according to a third embodiment. Note that components the same as those of the first embodiment are assigned the same notations and their explanations are omitted.

[0050]

In the first embodiment, an explanation was given of an example wherein the thicknesses of the gate insulating films of the transistor Tr1 and the transistor Tr2 were the same. In the third embodiment, as shown in FIG. 9, use is also made of separate formation of gate insulating films so that the physical thickness of the gate insulating film 3-1 of the high withstand voltage use transistor Tr1 becomes thicker than the gate insulating film 3-2 of the transistor Tr2.

[0051]

In the above semiconductor device according to the present embodiment, the physical thickness of the gate insulating film 3-1 of the high withstand voltage use transistor Tr1 supplied with high source voltage is

formed thicker than the gate insulating film 3-2 of the transistor Tr2. Therefore, combined with use of the depletion of the gate electrode 4a, the effective thickness of the gate insulating film can be thicker. Further, by forming gate insulating films having two different types of thickness by separate formation of gate insulating films and further utilizing depletion of the gate electrode 4a, it is possible to form gate insulating films having three types of electrical effective thickness. For the rest, similar effects are exhibited as with the first embodiment.

[0052]

Next, a method of producing a semiconductor device according to the present embodiment will be described with reference to FIG. 10 to FIG. 13. In the present embodiment, a step of separate formation of gate insulating films is performed before the step shown in FIG. 2(a) in the first embodiment.

[0053]

That is, as shown in FIG. 10(a), a semiconductor substrate 1 wherein active regions are determined by an element-isolation insulating film 2 formed by LOCOS or STI is formed with a gate insulating film 3-1 of silicon oxide by heat oxidation.

[0054]

Next, as shown in FIG. 10(b), only the transistor region where a thick gate insulating film is required is masked using a resist R6, then as shown in FIG. 10(c), the film is wet-etched using a hydrofluoric acid solution etc. to remove all of the parts of the gate insulating film 3-1 with no resist. After this, the resist R6 is removed.

[0055]

Next, as shown in FIG. 11(d), a second heat oxidation is performed. Due to this, the semiconductor substrate 1 stripped of the gate insulating film 3-1 is formed with a gate insulating film 3-2 by the second heat oxidation, whereby the existing gate insulating film 3-1 is made thicker. Note that the total oxide film thickness due to the two heat oxidations does not become the simple sum, so for the first heat oxidation, the thickness giving the desired thickness as the total is calculated in reverse and suitable heat oxidation performed. That is, when the first heat oxidation forms a gate insulating film 3-1 of for example 4 nm and the second heat oxidation forms a gate insulating film 3-2 of 2 nm, the thickness of the gate insulating film 3-1 becomes for example about 5 nm by the two heat oxidations.

[0056]

The following steps are similar to the steps from

FIG. 2(b) explained in the first embodiment. That is, as shown in FIG. 11(e), an amorphous silicon film 4-1 is formed on the gate insulating films 3-1 and 3-2. The thickness of the silicon film 4-1 is made for example about 50 to 200 nm. Next, gate ions are implanted for forming an n+ electrode. The gate ion implantation condition is implantation of for example P by an implantation energy of 20 keV and a dosage of 1 x 1015 cm-2. The dosage at this time is made a low concentration further facilitating gate depletion suitable for a element for which a thick gate insulating film is required such as a high withstand voltage use transistor Tr1.

[0057]

Next, as shown in FIG. 12(f), a resist R7 opening at the region including the gate electrode of the transistor Tr2 for which the highest performance is sought is patterned, then additional gate ions are implanted using this resist R7 as a mask. Due to this, a silicon film 4-2 containing an impurity at a high concentration is formed. This additional gate ion implantation is implantation of for example P at an implantation energy of 20 keV and a dosage of 3 x 1015 cm-2. The dosage at this time is set to one of a sufficiently high concentration for making gate depletion difficult so that the electrical effective

thickness of the gate insulating film required of the transistor Tr2 from which the highest performance is sought does not become thicker. The resist R7 is removed, then the implanted impurity is activated by heat treatment. Due to the heat treatment, amorphous silicon films 4-1 and 4-2 become polycrystalline silicon.

[0058]

Next, as shown in FIG. 12(g), the parts for forming the gate electrodes of the transistors Tr1 and Tr2 are masked by a resist R8, then, as shown in FIG. 13(h), the silicon films 4-1 and 4-2 are dry-etched using the resist R8 as a mask. After that, the resist R8 is removed. Due to this, a gate electrode 4a of the silicon film 4-1 containing an impurity at a low concentration and a gate electrode 4b of the silicon film 4-2 containing an impurity at a high concentration by two ions implantations are formed.

[0059]

Next, as shown in FIG. 13(i), an n-type impurity, for example, P, is implanted at a low concentration using the gate electrodes 4a and 4b as a mask to form n- semiconductor regions 6a in the semiconductor substrate 1. By depositing and etching back for example a silicon oxide film, sidewall insulating films 5 are formed at the side parts of the gate electrodes 4a and 4b.

[0060]

As the following steps, an n-type impurity, for example, P, is implanted at a high concentration using the gate electrodes 4a and 4b and the sidewall insulating films 5 as a mask to form n+ semiconductor regions 6b. By this, source/drain regions 6 having LDD structures are formed. By removing the gate insulating films 3-1 and 3-2 on the source/drain regions 6, the semiconductor device shown in FIG. 5 is produced.

[0061]

According to the method of producing a semiconductor device of the present embodiment, since the gate electrode 4a of the high withstand voltage use transistor Tr1 is formed by using the silicon film 4-1 by a first low concentration gate ion implantation plus use of the gate insulating film 3-1 of thick film formed by separation formation of gate insulating films, the electrical effective thickness required from the gate insulating films can be made thicker than the first embodiment. Therefore, the reliability of the transistors can be raised. Further, by separately forming gate insulating films with two different types of physical thicknesses by for example separation formation of the gate insulation films and utilizing depletion of the gate electrode 4a, it is possible to efficiently

simultaneously produce three types of transistors on the same substrate while maintaining the capability of the transistors. Otherwise, the same effects as in the first embodiment can be obtained.

[0062]

Fourth Embodiment

FIG. 14 is a cross-sectional view of a semiconductor device according to a fourth embodiment. Note that components the same as those of the second embodiment are assigned the same notations and their explanations are omitted.

[0063]

In the second embodiment, the explanation was given of the example of the same thicknesses of the gate insulating film of the transistor Tr2 and the capacitive insulating film of the capacitor Ca. In the present embodiment, as shown in FIG. 14, separation formation of the gate insulating films is used so that the physical thickness of the capacitive insulating film 3-1c of the high withstand voltage use capacitor Ca is formed thick compared with the gate insulating film 3-2b of the transistor Tr2.

[0064]

In the above semiconductor device according to the present embodiment, the physical thickness of the

capacitive insulating film 3-1c of the high withstand voltage use capacitor Ca supplied with high source voltage is formed thicker than the gate insulating film 3-2b of the transistor Tr2. Therefore, along with utilization of depletion of the upper electrode 4c of the capacitor, it is possible to further increase the electrical effective thickness required of a capacitive insulating film. Otherwise, effects similar to those of the first embodiment are exhibit.

[0065]

Next, a method of producing a semiconductor device according to the present embodiment will be described with reference to FIG. 15 to FIG. 19. In the present embodiment, the step of separate formation of the gate insulating films is performed before the steps of FIG. 6(a) and FIG. 6(b) in the second embodiment.

[0066]

That is, as shown in FIG. 15(a), a semiconductor substrate 1 wherein active regions are determined by an element-isolation insulating film 2 formed by LOCOS or STI is formed with a sacrificial film 8 of silicon oxide by heat oxidation. The thickness of the sacrificial film 8 is for example about 8 nm. Next, a resist R9 opening at the capacitor formation region is patterned. By implanting ions using this resist R9 as a mask, a bottom

electrode 7 is formed. The dosage at this time is one sufficient for conversion to an n+ or p+ form, but not increasing the gate leakage current or increasing the crystal defects and lowering reliability. For example, As ions are implanted at an implantation energy of 70 keV and a dosage of 1 x 1015 cm-2.

[0067]

Next, as shown in FIG. 15(b), the resist film R9 is removed and the sacrificial film 8 is removed by a hydrofluoric acid solution, then the insulating film 3-1c for forming the capacitive insulating film of the capacitor Ca is formed by heat oxidation.

[0068]

Next, as shown in FIG. 16(c), only the capacitor region where a thick gate insulating film is required is masked using a resist R10, then as shown in FIG. 16(d), the film is wet-etched using a hydrofluoric acid solution etc. to remove all of the parts of the gate insulating film 3-1c with no resist. After this, the resist R10 is removed.

[0069]

Next, as shown in FIG. 17(e), a second heat oxidation is performed. Due to this, the semiconductor substrate 1 stripped of the gate insulating film 3-1 is formed with a gate insulating film 3-2 by the second heat

oxidation, whereby the existing gate insulating film 3-1c is made thicker. Note that as explained in the third embodiment, the total oxide film thickness due to the two heat oxidations does not become the simple sum, so for the first heat oxidation, the thickness giving the desired thickness as the total is calculated in reverse and suitable heat oxidation performed.

[0070]

The following steps are similar to the steps from FIG. 6(b) explained in the second embodiment. That is, as shown in FIG. 17(f), an amorphous silicon film 4-1 is formed on the gate insulating film 3-2b and the capacitive insulating film 3-1c. The thickness of the silicon film 4-1 is made for example about 50 to 200 nm. Next, ions are implanted for forming an n+ electrode. The ion implantation is implantation of for example P by an implantation energy of 20 keV and a dosage of 1 x 1015 cm-2. The dosage at this time is made a low concentration further facilitating gate depletion suitable for an element for which a thick capacitive insulating film is required such as a high power source voltage capacitor Ca.

[0071]

Next, as shown in FIG. 18(g), a resist R11 opening at the region including the gate electrode of the transistor Tr2 from which a high performance is sought is

patterned. Using this resist R11 as a mask, additional ions are implanted. Due to this, a silicon film 4-2 containing an impurity at a high concentration is formed. The detailed conditions of the additional gate ion implantation are similar to those of the additional gate ion implantation of the first embodiment. The resist R11 is removed, then the implanted impurity is activated by heat treatment. Due to this heat treatment, the amorphous silicon films 4-1 and 4-2 become polycrystalline silicon.

[0072]

Next, as shown in FIG. 18(h), the part for forming the gate electrode of the transistor Tr2 and the part for forming the upper electrode of the capacitor Ca are masked by a resist R12, then, as shown in FIG. 18(i), the silicon films 4-1 and 4-2 are dry-etched using the resist R12 as a mask. After that, the resist R12 is removed. Due to this, the upper electrode 4c of the silicon film 4-1 containing an impurity at a low concentration and the gate electrode 4b of the silicon film 4-2 formed by two ion implantations and containing an impurity in high concentration of the impurity are formed.

[0073]

Next, as shown in FIG. 19(j), in the state masking the capacitor formation region by a resist, an n-type impurity, for example P, is implanted at the transistor

formation region at a low concentration using the gate electrode 4b as a mask to form an n- semiconductor region 6a. The resist is removed, then for example a silicon oxide film is deposited and etched back to form sidewall insulating films 5 at the side parts of the gate electrode 4b.

[0074]

As the following steps, in the state masking the capacitor formation region by a resist, an n-type impurity, for example P, is implanted at the transistor formation region at a high concentration using the gate electrode 4b and the sidewall insulating film 5 as a mask to form an n+ semiconductor region 6b. Due to this, a source/drain region 6 having an LDD structure is formed. The exposed parts of the insulating films 3-2b and 3-1c are removed to form the gate insulating film 3-2b of the transistor Tr2 and the capacitive insulating film 3-1c of the capacitor Ca, whereby the semiconductor device shown in FIG. 7 is produced.

[0075]

According to the method of producing a semiconductor device according to the present embodiment, by separately preparing insulating films for forming the gate insulating film and capacitive insulating film and utilizing depletion of the upper electrode, it is

possible to make electrical effective thickness of the capacitor thicker than the second embodiment. Therefore, it is possible to form a capacitor having the desired capacity without increasing the leakage current due to crystal defects caused by damage received at the time of high concentration ion implantation for forming the bottom electrode and without a decline in the reliability.

[0076]

The present invention is not limited to the above embodiments. In the embodiments, the explanation was given with reference to an example of simultaneously forming the transistor Tr1 and the transistor Tr2 having different electrical effective thicknesses required of the gate insulating film and an example of simultaneously forming the transistor Tr2 and the capacitor, but it is also possible to simultaneously form three electronic elements of the transistor Tr1, the transistor Tr2, and the capacitor Ca. Further, the explanation was given of an example of the configuration of transistors and capacitors, but the invention is not limited to this. The sidewall insulating film etc. may be omitted. In addition, the numerical values and materials mentioned in the embodiments are examples. The invention is not limited to this. Various modifications and others may be applicable within the scope of the present invention.

[0077]

[Effect of the Invention]

According to the semiconductor device of the present invention, it is possible to secure electrical effective thicknesses required for insulating films of electronic circuit elements by using depletion of electrodes of the electronic circuit elements even if the physical thicknesses of the insulating films are not different.

[0078]

According to the method of producing a semiconductor device of the present invention, it is possible to secure electrical effective thicknesses required for gate oxide films of transistors and capacitive insulating films of capacitors while keeping down the increase in number of steps due to the selective formation of insulating films with physically different thicknesses.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1]

FIG. 1 is a cross-sectional view of an example of a semiconductor device according to a first embodiment.

[Fig. 2]

FIGS. 2(a) to 2(b) are cross-sectional views of steps of producing a semiconductor device according to the first embodiment.

[Fig. 3]

FIGS. 3(c) to 3(d) are cross-sectional views of steps of producing a semiconductor device according to the first embodiment.

[Fig. 4]

FIGS. 4(e) to 4(f) are cross-sectional views of steps of producing a semiconductor device according to the first embodiment.

[Fig. 5]

FIG. 5 is a cross-sectional view of an example of a semiconductor device according to a second embodiment.

[Fig. 6]

FIGS. 6(a) to 6(b) are cross-sectional views of steps of producing a semiconductor device according to the second embodiment.

[Fig. 7]

FIGS. 7(c) to 7(d) are cross-sectional views of steps of producing a semiconductor device according to the second embodiment.

[Fig. 8]

FIGS. 8(e) to 8(f) are cross-sectional views of steps of producing a semiconductor device according to the second embodiment.

[Fig. 9]

FIG. 9 is a cross-sectional view of an example of a semiconductor device according to a third embodiment.

[Fig. 10]

FIGS. 10(a) to 19(c) are cross-sectional views of steps of producing a semiconductor device according to the third embodiment.

[Fig. 11]

FIGS. 11(d) to 11(e) are cross-sectional views of steps of producing a semiconductor device according to the third embodiment.

[Fig. 12]

FIGS. 12(f) to 12(g) are cross-sectional views of steps of producing a semiconductor device according to the third embodiment.

[Fig. 13]

FIGS. 13(h) to 13(i) are cross-sectional views of steps of producing a semiconductor device according to the third embodiment.

[Fig. 14]

FIG. 14 is a cross-sectional view of an example of a semiconductor device according to a fourth embodiment.

[Fig. 15]

FIGS. 15(a) to 15(b) are cross-sectional views of steps of producing a semiconductor device according to the fourth embodiment.

[Fig. 16]

FIGS. 16(c) to 16(d) are cross-sectional views of

steps of producing a semiconductor device according to the fourth embodiment.

[Fig. 17]

FIGS. 17(e) to 17(f) are cross-sectional views of steps of producing a semiconductor device according to the fourth embodiment.

[Fig. 18]

FIGS. 18(g) to 18(h) are cross-sectional views of steps of producing a semiconductor device according to the fourth embodiment.

[Fig. 19]

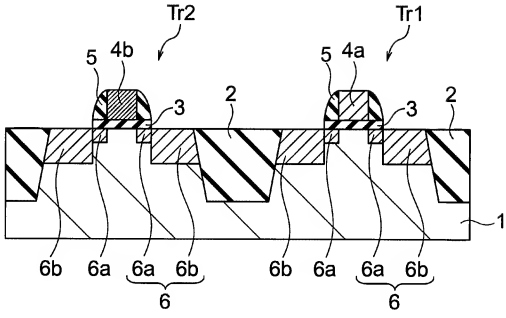
FIGS. 19(i) to 19(j) are cross-sectional views of steps of producing a semiconductor device according to the fourth embodiment.

[Description of References]

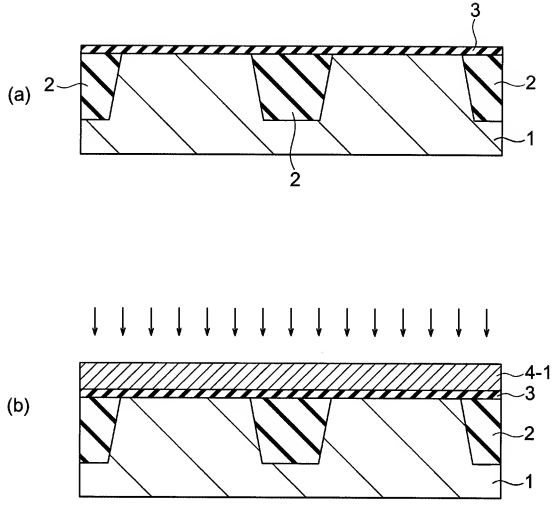
1...semiconductor substrate; 2...element-isolation insulating film; 3, 3b, 3-1, 3-2, 3-2b...gate insulating film; 3c,3-1c...capacitive insulating film; 4a, 4b...gate electrode; 4c...upper electrode; 4-1, 4-2...silicon film; 5...sidewall insulating film; 6...source/drain regions; 6a...n- semiconductor region; 6b...n+ semiconductor region; 7...lower electrode; 8...sacrificial film; Tr1, Tr2...transistor; Ca...capacitor; R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12...resist

[Name of Document] Figures

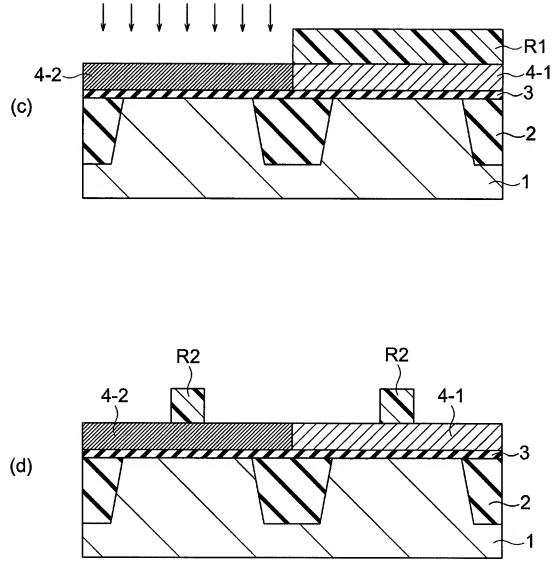
[FIG.1]



[FIG.2]

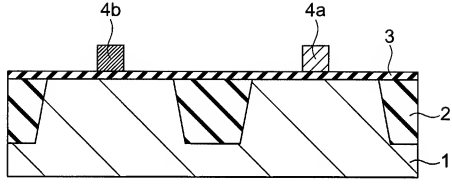


[FIG.3]

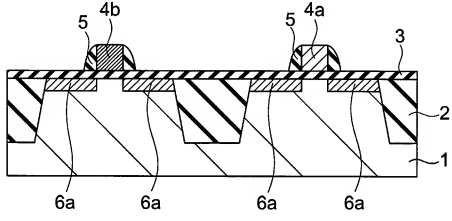


[FIG.4]

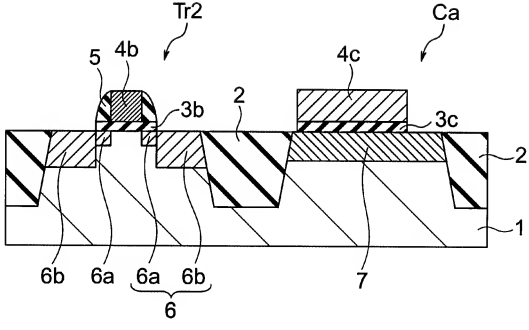
(e)



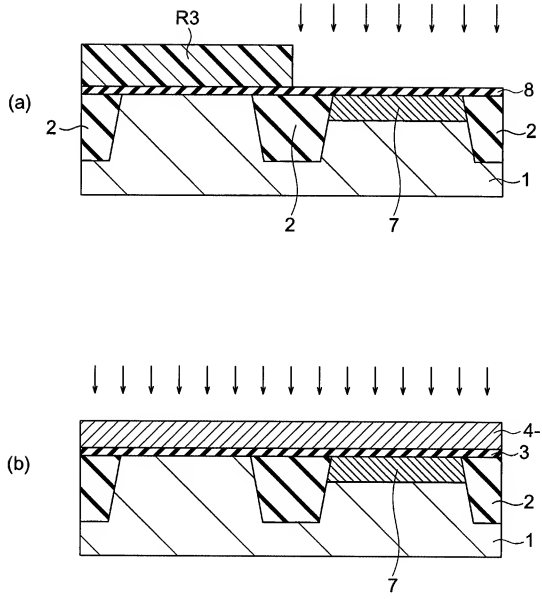
(f)



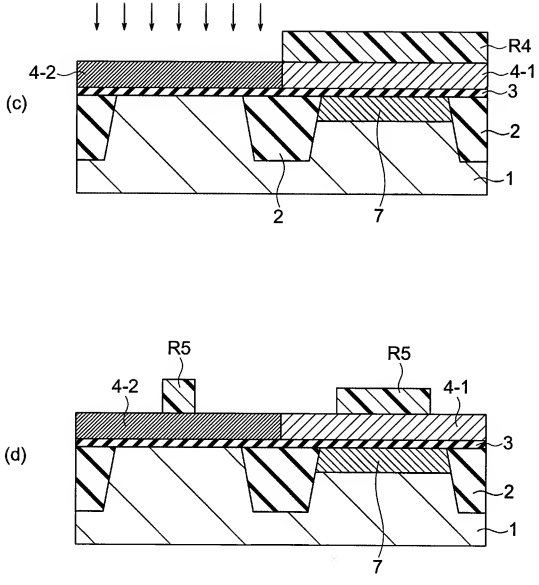
[FIG.5]



[FIG. 6]

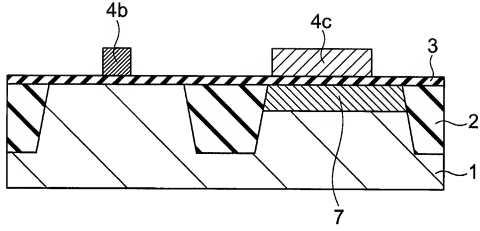


[FIG.7]

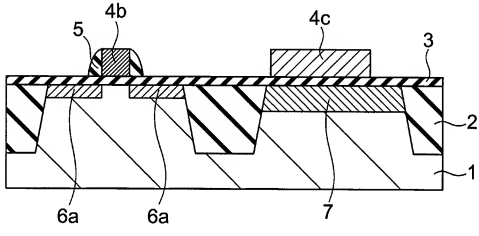


[FIG.8]

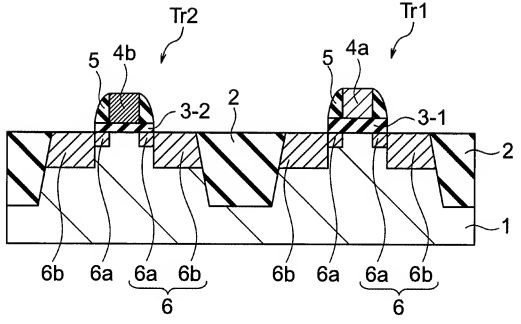
(e)



(f)

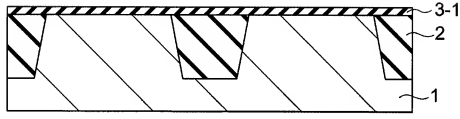


[FIG.9]

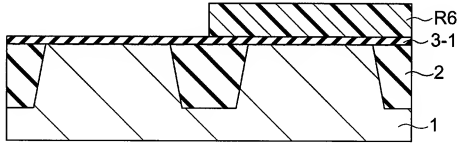


[FIG.10]

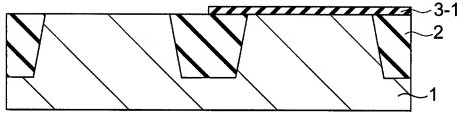
(a)



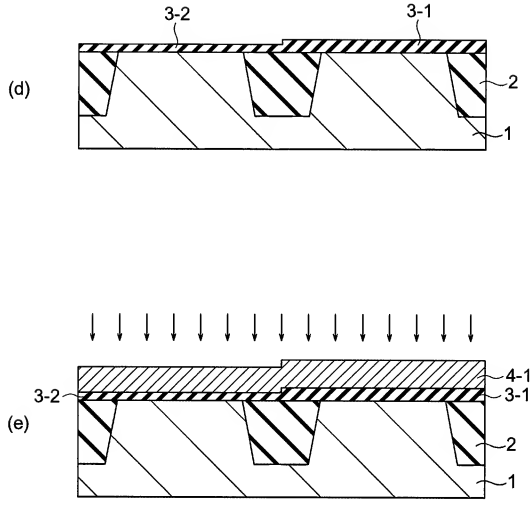
(b)



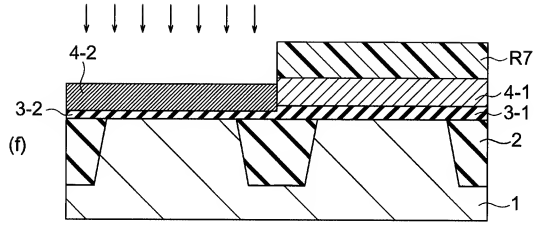
(c)

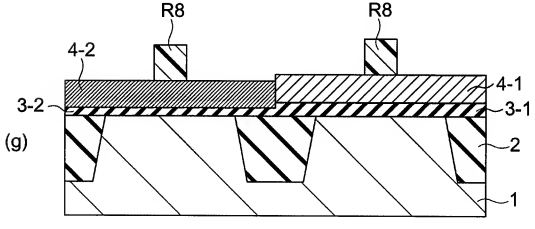


[FIG.11]



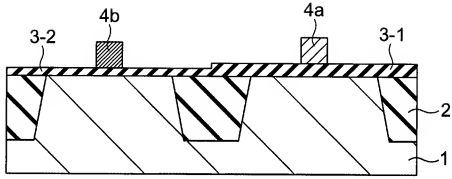
[FIG.12]



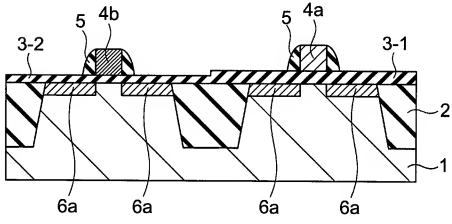


[FIG.13]

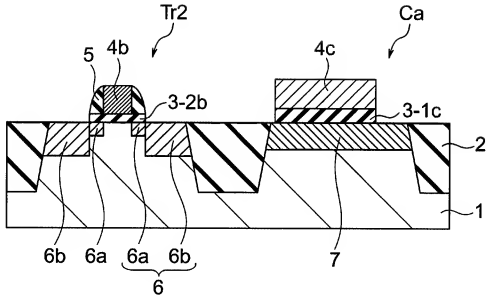
(h)



(i)

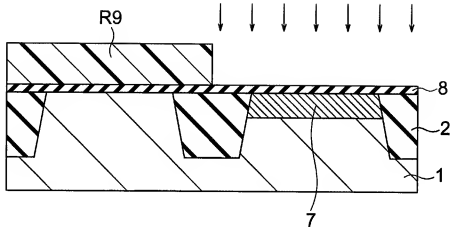


[FIG.14]



[FIG.15]

(a)



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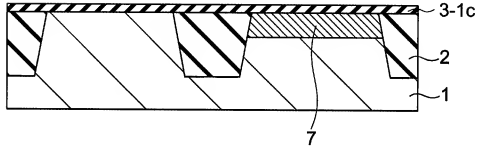
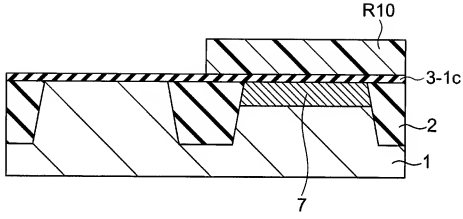
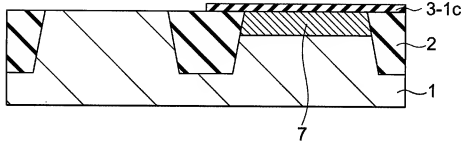


[FIG.16]

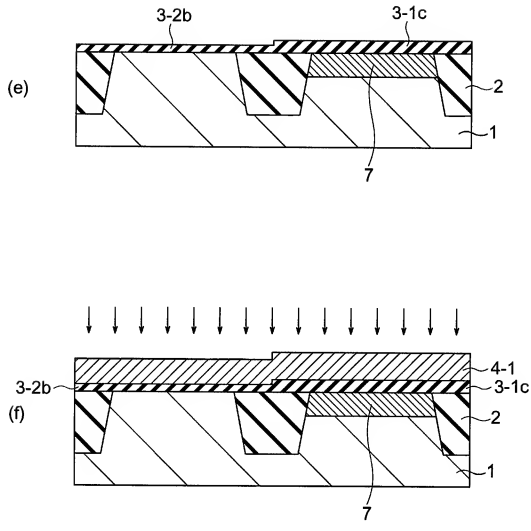
(c)



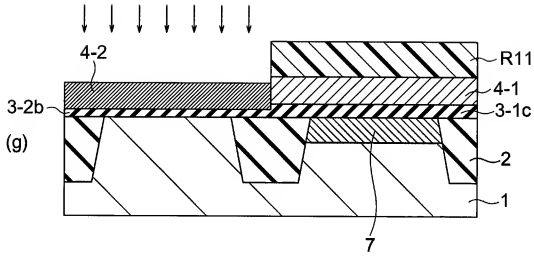
(d)

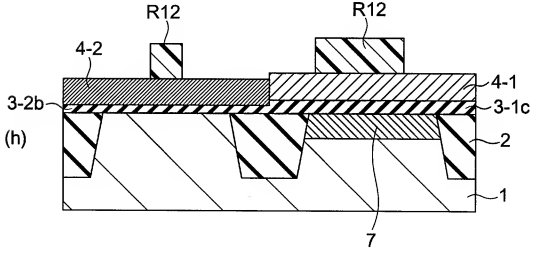


[FIG.17]



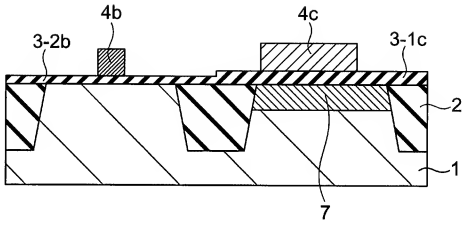
[FIG.18]



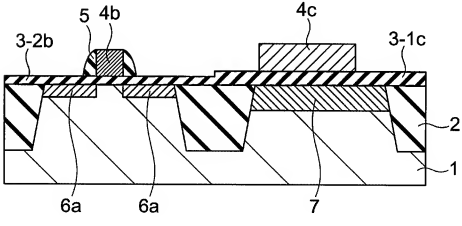


[FIG.19]

(i)



(j)



[NAME OF DOCUMENT] Abstract

[ABSTRACT]

[PROBLEM] To provide a semiconductor device and a method of producing thereof, cable of securing electrical effective thicknesses required for insulating films of electronic elements by using depletion of electrodes of the electronic elements even if the physical thicknesses of the insulating films are not different.

[MEANS FOR SOLUTION] Gate electrodes of high withstand voltage use transistors to which high power source voltages are supplied contain an impurity at a relatively low concentration, so the gate electrodes are easily depleted at the time of application of the gate voltage; depletion of the gate electrodes is equivalent to increasing the thickness of the gate insulating films; the electrical effective thicknesses required of the gate insulating films can be made thicker; and the gate electrodes of high performance transistors for which a high speed and large drive current are required do not contain an impurity at a high concentration where depletion of the gate electrodes will not occur, so the electrical effective thickness of the gate insulating films is kept thin.

[SELECTED DRAWING] Fig. 1